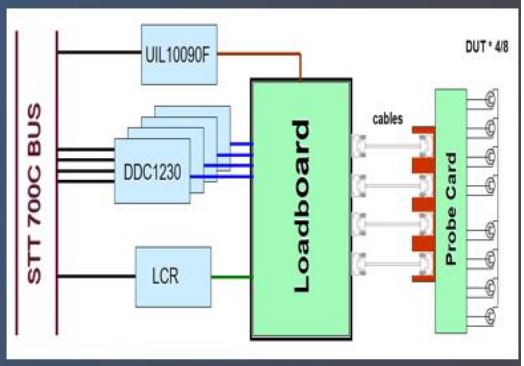
Mosfet/IGBT DC+UIL+CS/RS wafer test solution (4/8/16/32… sites)

Mosfet/IGBT DC+UIL+CS/RS 8 sites wafer test Solution

- **Hardware Config**
  4*DDC1230
  1*UIL10090F
  1*LCR module
- **Advantages:**
  Easy setup
  Physical fool-proof design
  High UPH



Assuming DC test time=100ms,prober index time=300ms,uil single mode=50ms,cgrg single mode=35ms

CP Multi-sites	Config	Test time per touch down	Gross dies 40K test use time	UPH
4sites DC+UIL+CGRG	2DDC+1UIL+1LCR	200(dc)+200(eas)+140(rg)=0.54S	40000/4*(0.54+0.3)=2.3h	17.4K/h
4sites DC+UIL+CGRG	4DDC+1UIL+1LCR	100(dc)+200(eas)+140(rg)=0.44S	40000/4*(0.44+0.3)=2.05h	19.5K/h
8sites DC+UIL+CGRG	4DDC+1UIL+1LCR	200(dc)+400(eas)+280(rg)=0.88S	40000/8*(0.88+0.3)=1.63h	24.5K/h
8sites DC+UIL	4DDC	200(dc)+400(eas)=0.6S	40000/8*(0.6+0.3)=1.25h	32.0K/h
8sites DC	4DDC	200=0.2S	40000/8*(0.2+0.3)=0.69h	57.9K/h
16sites DC	8DDC	200=0.2S	40000/16*(0.2+0.3)=0.34h	117K/h
32sites DC	8DDC	400=0.4S	40000/32*(0.4+0.3)=0.24h	166K/h

Wafer Test Solution -- multisite AC+DC test

1. DC (4/8/16/32 even 64 sites…)
2. DC+AC(UIL+Rg etc.,), 4 /8 sites…
3. Multisite for Non-Baking Non-Grinding wafer, 4/8 sites…

Highly integrated and higher UPH of SineTest's wafer test solution, also has space saving advantage, finally help the customers to achieve the lowest cost of test.