实用案例: Mosfet/IGBT8/16/32/64 工位晶圆测试方案，业内最高 UPH！

CP MOS/IGBT Support DC+UIL+CS/RS 8sites Test

- **Hardware Config**

4 or 8*DDC1020/DDC1230
1*UIL10090E/J/F
1*LCR module
8sites Loadboard/Cables

8sites
UIS+RG+DC.c

- **Highlight**

Easy setup
Physical fool-proof design（物理防呆），专有设计有效避免高压打火

Assuming DC test time=100ms,prober index time=300ms,uil single mode=50ms,cgrg single mode=35ms				
CP Multi-sites	**Config**	**Test time per touch down**	**Gross dies 40K test use time**	**UPH(k/h)**
4sites DC+UIL+CGRG	2DDC+1UIL+1LCR	200(dc)+200(eas)+140(rg)=0.54S	40000/4*(0.54+0.3)=2.3h	17.4K/h
4sites DC+UIL+CGRG	4DDC+1UIL+1LCR	100(dc)+200(eas)+140(rg)=0.44S	40000/4*(0.44+0.3)=2.05h	19.5K/h
8sites DC+UIL+CGRG	4DDC+1UIL+1LCR	200(dc)+400(eas)+280(rg)=0.88S	40000/8*(0.88+0.3)=1.63h	24.5K/h
8sites DC+UIL	4DDC+1UIL	200(dc)+400(eas)=0.6S	40000/8*(0.6+0.3)=1.25h	32.0K/h
8sites DC	4DDC	200=0.2S	40000/8*(0.2+0.3)=0.69h	57.9K/h
16sites DC	8DDC	200=0.2S	40000/16*(0.2+0.3)=0.34h	117K/h
32sites DC	8DDC	400=0.4S	40000/32*(0.4+0.3)=0.24h	166K/h

CP MOS Solution -- Multisite DC+EAS+RG/CS Test

Mosfet圆片DC+EAS+RG/CS交流多工位测试方案

1. DC (1/2/4/8/16/32 even 64 sites…)

2. DC+EAS+RG/CG (1/2/4/8 sites…)

3. D2D Test—— Multisite for Non-Baking Non-Grinding wafer（多工位不背金不减薄圆片并测能力）

赛英特技术的方案，集成度高，UPH 高，占地面积少，无杂乱的外置测试盒，是新一代的分立器件晶圆测试方案。